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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/945,247	08/31/2001	Seiichiro Higashi	9319T-000281	1294
27572	7590 04/18/2003			
HARNESS, DICKEY & PIERCE, P.L.C.			EXAMINER	
P.O. BOX 828 BLOOMFIEL	B D HILLS, MI 48303		SOWARD, IDA M	
			ART UNIT	PAPER NUMBER
			2822	
			DATE MAILED: 04/18/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)		
		09/945,247	HIGASHI ET AL.		
•	Office Action Summary	Examiner	Art Unit		
		Ida M Soward	2822		
	The MAILING DATE of this communication ap	opears on the cover sheet with the	correspondence address		
THE I - Exter after - If the - If NO - Failu - Any r	ORTENED STATUTORY PERIOD FOR REP MAILING DATE OF THIS COMMUNICATION raisons of time may be available under the provisions of 37 CFR 1 SIX (6) MONTHS from the mailing date of this communication. period for reply specified above is less than thirty (30) days, a reperiod for reply is specified above, the maximum statutory perior to reply within the set or extended period for reply will, by statuely received by the Office later than three months after the mailing datent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may a reply be tile ply within the statutory minimum of thirty (30) day d will apply and will expire SIX (6) MONTHS from the cause the application to become ABANDONE	mely filed ys will be considered timely. the mailing date of this communication. ED (35 U.S.C. § 133).		
1)⊠	Responsive to communication(s) filed on 03	March 2003 .			
2a)□		his action is non-final.			
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims					
4)🛛	Claim(s) 1-16 is/are pending in the application	on.			
	4a) Of the above claim(s) is/are withdr	awn from consideration.			
5)	Claim(s) is/are allowed.				
6)⊠	Claim(s) <u>1-16</u> is/are rejected.				
7)	Claim(s) is/are objected to.				
8)	Claim(s) are subject to restriction and/	or election requirement.			
Applicati	on Papers				
9) 🗌 -	Γhe specification is objected to by the Examin	er.			
10) 🔲 🗀	Γhe drawing(s) filed on is/are: a)∏ acc	epted or b) \square objected to by the Exa	miner.		
	Applicant may not request that any objection to t				
11) 🔲 🛚	The proposed drawing correction filed on		oved by the Examiner.		
	If approved, corrected drawings are required in r	• •			
•	The oath or declaration is objected to by the E	xaminer.			
•	nder 35 U.S.C. §§ 119 and 120				
13)	Acknowledgment is made of a claim for foreign	gn priority under 35 U.S.C. § 119(a	a)-(d) or (f).		
a)[☐ All b) ☐ Some * c) ☐ None of:				
	1. Certified copies of the priority documer	nts have been received.			
	2. Certified copies of the priority documer	nts have been received in Applicati	ion No		
	3. Copies of the certified copies of the pricapplication from the International B ee the attached detailed Office action for a lis	ureau (PCT Rule 17.2(a)).	-		
14)∐ A	cknowledgment is made of a claim for domes	tic priority under 35 U.S.C. § 119(e) (to a provisional application).		
15) 🗌 A	The translation of the foreign language processions. The translation of the foreign language processions.	• •			
Attachment					
2) Notice	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal	y (PTO-413) Paper No(s) Patent Application (PTO-152)		
S. Patent and Tr PTO-326 (Re		Action Summary	Part of Paper No. 13		

DETAILED ACTION

This Office Action is in response to Applicants' remarks filed March 3, 2003.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5-8 and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (5,970,384) in view of Grill et al. (US 2002/0037442 A1) and Yamazaki et al. (US 2002/0034863 A1).

Yamazaki et al. (5,970,384) teach a method for the fabrication of a field-effect transistor comprising the steps of: forming a semiconductor layer **704** serving as an active layer on a substrate **701**; forming a stage gate insulating film **705** on the semiconductor layer; heat treating the gate insulating film in an N₂O atmosphere (col. 15, lines 7-37) (Figure 7E, col. 12, lines 40-67). Yamazaki et al. (5,970,384) further teach the gate insulating film formed by plasma CVD method using a TEOS gas (col. 5, lines 45-58). However, Yamazaki et al. (5,970,384) fail to teach setting the substrate temperature at no higher than 100°C and heat-treating the gate insulating film in an atmosphere containing water. Grill et al. teach setting the substrate temperature at between about 25°C and about 400°C, which is in the range of no higher than or no less

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than 100°C. (page 2, paragraph [0022]). Yamazaki et al. (US 2002/0034863 A1) teach heat-treating in an atmosphere containing water (page 13, paragraph [0269]). Since Yamazaki et al. (5,970,384), Grill et al. and Yamazaki et al. (US 2002/0034863 A1) are from the same field of endeavor (method of manufacturing semiconductors), the purpose disclosed by Yamazaki et al. (US 2002/0034863 A1) would have been recognized in the pertinent art of Yamazaki et al. (5,970,384) and Grill et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method for the fabrication of a field-effect transistor of Yamazaki et al. (5,970,384) by incorporating the substrate temperature of Grill et al. and the atmosphere containing water of Yamazaki et al. (US 2002/0034863 A1) to obtain a semiconductor device having an excellent performance (page 13, paragraphs [0269]-[0273]).

Claims 3-4 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (5,970,384), Grill et al. (US 2002/0037442 A1) and Yamazaki et al. (US 2002/0034863 A1) as applied to claims 1 and 7-8 above, and further in view of An et al. (US 6,245,618 B1).

Yamazaki et al. (5,970,384), Grill et al. and Yamazaki et al. (US 2002/0034863 A1) teach all mentioned in the rejection above. However, Yamazaki et al. (5,970,384), Grill et al. and Yamazaki et al. (US 2002/0034863 A1) fail to teach conducting a process while cooling a substrate. An et al. teach conducting a process while cooling a substrate (col. 1, lines 46-56). Since Yamazaki et al. (5,970,384), Grill et al., Yamazaki

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et al. (US 2002/0034863 A1) and An et al. are from the same field of endeavor (method of manufacturing semiconductors), the purpose disclosed by An et al. would have been recognized in the pertinent art of Yamazaki et al. (5,970,384), Grill et al. and Yamazaki et al. (US 2002/0034863 A1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method for the fabrication of a field-effect transistor of Yamazaki et al. (5,970,384), the substrate temperature of Grill et al. and the atmosphere containing water of Yamazaki et al. (US 2002/0034863 A1) by incorporating cooling a substrate of An et al. to reduce junction leakage current (col. 1, lines 46-56).

Response to Arguments

Applicant's remarks filed 03-03-03 have been fully considered but they are not persuasive.

In response to the remarks concerning Grill et al., Grill et al. is not being relied upon for the multiphase film being deposited on the substrate. Grill et al. is being relied upon because it's a method of forming a semiconductor structure whose substrate temperature is set at a range of no higher than or no less than 100 degrees C. In regard to the substrate temperature, it is not inventive to point out a particular range of conditions or optimum working ranges if what is involved is nothing more than skill of mechanic and exercise of patient experimentation; pantentee simply cannot designate a range in a known process and maintian a monopoly on processes within that range on

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the grounds that it produces optimum results. Duplan Corp. v. Derring Milliken, Inc., 444 F.Supp. 648 (D.C. S.C. 1977).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to a method for fabricating field effect transistors:

Ono (US 6,300,239 B1)

Saito et al. (4,889,817)

Satake et al. (US 6,208,002 B1)

Yamazaki et al. (US 6,261,877 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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ims April 16, 2003

ANNIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800